In the Specification:

Please replace the following paragraphs in the specification:

Page 4, paragraph from lines 3-16.

Another embodiment includes a voltage controlled oscillator using two such delay units in series. The oscillator has a first delay unit and a second delay unit, each having four transistors. In both units, a first and a second transistor are connected as a first amplifier, a two-transistor positive amplifier, with the gate of the first transistor connected to the source of the second transistor, and the source of the second transistor connected to the gate of the first transistor. There is a second amplifier having a third and a fourth transistor, the drains of the third and fourth transistors connector to the sources of the first and third transistors respectively, the connections forming outputs of each of the two delay units. The outputs of the first delay unit are connected to gates of the second amplifier of the second delay unit, and the outputs of the second delay unit are connected to gates of the second amplifier of the first delay unit. A ~~control input and~~ power supply voltage ~~are~~ is then connected to the drains of the first amplifiers.

Please replace the paragraph on p. 5, lines 5-15 with:

Fig. 3a depicts a delay unit 30 having a positive feedback amplifier 50, a linear amplifier 52, and a differential output voltage. Transistors 56 and 58 are PMOS transistors and are connected back-to-back in the sense that the gate of each transistor is tied to the drain of the other transistor. A supply voltage ~~and control voltage~~ V_{pos}, along with its return or a negative supply, V_{neg}, control the amplifier. The drains of the transistors 56, 58 are connected to a linear amplifier 52, and particularly to the drains of NMOS transistors 60 and 62. A differential voltage signal is connected to the gates of the linear amplifier transistors 60, 62.

The voltage output, now having a delay determined by the supply ~~and control~~ voltage and V_{in}, is taken from the V_{out} terminals, the joint outputs 68 of the positive feedback amplifier 50 and the input signal to the linear amplifier 52.

Please replace the paragraph between pp. 5 and 6, from p. 5, line 26, to p. 6, line 9, with:

In this configuration, the positive feedback amplifier 50 is wired so that the transistors 56, 58 act as pull-up transistors, while the linear amplifier 52 acts as pull-down transistors. Thus, the delay unit is fully differential, with the positive feedback portion 50 coupling the outputs of the linear (differential delay) amplifier 52. The circuit works by forcing both outputs of the delay stage to have 180 degrees phase difference. With this design, and that of Fig. 4a, below, the delay unit is able to use nearly all of the available positive input voltage, that is, there is a large voltage swing, from V_{neg} nearly to the V_{pos} input ~~and control~~ voltage. This allows the delay unit to have a larger range of delay outputs for the user and improves the ratio of oscillation signal to noise. This design also provides for nearly symmetric rise and fall times of the phase outputs of the delay units, whether a single unit or several in series to form a voltage oscillator or frequency synthesizer.

Please replace the paragraph on p. 8, lines 3-16, with:

Fig. 5 depicts another embodiment, in which two identical delay units 82 and 84 are connected in series as shown, to form a voltage controlled oscillator 80 (VCO) or voltage-to-frequency converter. In Fig. 5, delay unit 82 depicts a first stage of the VCO 80, while delay unit 84 depicts the second stage, wherein the only difference between the two stages is the manner of connecting their outputs. First delay unit 82 and second delay unit 84 both include a first (feedback) amplifier 50 and a second (linear) amplifier 52. First amplifiers 50

include PMOS transistors 86, 88, connected as positive feedback amplifiers, with a gate of one transistor tied to a drain of the other. Second amplifiers 52 include NMOS transistors 90, 92, connected as linear amplifiers, and with their drains connected to the drains of the first amplifiers 50 as an output signal. The use of the ~~control input and~~ positive supply voltage 94 both as a power source and as a control input takes advantage of the inherent advantages of CMOS technology, connecting to the sources of transistors 86 and 88 in delay units 82 and 84.

Please replace the paragraph that spans pp. 8-9, from p. 8, lines 17, to p. 9, line 2, with:

The control input to the positive terminals 94 is as shown, and a negative supply voltage (or ground) at terminal 96. The output phases of the respective feedback amplifiers 50 and linear amplifiers 52 are connected as shown at connections 68, in both the first and the second delay units 82, 84. Thus, the first and second amplifiers are connected, with the output of first stage phase 1 and phase 3 connected to the gates of the second phase linear amplifier. The output signal of the second stage unit is taken as shown, with output phase 2 connected to the gate of the linear amplifier transistor 90 of the first stage, and the output phase 4 connected to the gate of first stage transistor 92. The output signal of the VCO is taken from output terminals 99 as shown, wherein the frequency of the output signals will vary with the ~~control input and~~ positive supply voltage. The VCO functions by charging and discharging the inherent parasitic capacitance from its output nodes to positive or negative power nodes and also between different output nodes. The timing of the charging and discharging is dependent on the voltage inputs to the VCO 80 or voltage-to-frequency converter.